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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/036,550	12/21/2001	Robert E. Stengel	CM03422J	4633

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EXAMINER	
MOTTOLA, STEVEN J	
ART UNIT	**PAPER NUMBER**
2817	

DATE MAILED: 04/07/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/036,550	STENGEL ET AL.	
	Examiner	Art Unit	
	Steven J. Mottola	2817	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-29 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-29 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

Claims 1-29 are rejected under 35 U.S.C. 102(e) as being anticipted by Pavio et al.

Refer to fig. 1 for instance of Pavio et al. Treating the independent claims 1 and 12 first, an input signal INPUT may be read as the signal of interest claimed; the unlabeled input terminal may be read as the local or first node claimed. Then the inductors 30 may be read as the corresponding coupled elements of claim 12 defining nodes therebetween which define different transmission paths which will have different delays as in claim 1 (relative to the input node). The transistors 18 may be read as the transistive elements of claim 12 which provide output signals at nodes along an output line defined by inductances 22. The outputs are combined by inductances 22 (which may be read as the additive elements of claim 12) defining nodes therebetween that

may be read as the remote nodes claimed and to add the signals from the transistors in phase to produce an output that may be read on the destination signal of claim 12 at an output node. The setting step of claim 1 is met by the selection of components necessary to realize the circuit of fig. 1 of Pavio et al.; this will inherently set the delay and phase of each path. In regard to claims 2,3 and 13 the discussion at lines 45-53 of col. 2 of Pavio et al. indicates that the circuit of fig. 1 is integrated and broadbanded. Regarding claims 4-5, the delays/phases would inherently be set by whatever component values were selected, and thus be predetermined. Regarding claims 6,15,21 & 22, the inductances 30 & 22 of Pavio et al appear to all be the same, and regarding claims 7 & 14, each transistor amplifier appears the same so that the amplitudes should be equal. Regarding claim 8, the input in Pavio et al. appears to be from an external source (not shown). Regarding claims 9 and 17, parasitic noise is inherent when using transistors at the frequencies of interest to Pavio et al., and any noise that did not original at the input would inherently be combined out of phase. Regarding claim 16, the device of Pavio et al. are microwave amplifiers (col. 1, line 49) that may find use in transmitters Col. 1, lines 13-14); this meets the RF power amplifier application limitation of the claim. The inductors and transistors of Pavio et al. meet the limitations of claims 18-19, and the inductors 30 form an artificial line as in claim 20. The inductors 22 defining nodes therebetween appears to meet the limitations of claim 23 and the last inductor before the output terminal may be read as the power handling device identical to the additive elements (read on the inductors 22), and in re claim 25, identical with itself as well as the other inductors 22. Its other terminal is connected to the output in re

claim 26. While fig. 1 of Pavio et al. has been referenced as it is the simplest circuit shown the above rejection could also be applied using the more complicated circuit of fig. 3 of Pavio et al. Here pavio et al. disclose the use of a bridged tee output line arrangement meeting claim 27, as well as (unlabeled) supply choke meeting claims 28-29.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steven J. Mottola whose telephone number is 571-272-1766. The examiner can normally be reached on M-Th from 8 to 5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert J. Pascal, can be reached on 571-272-1766. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Steven J. Mottola
Primary Examiner